CMS8M35xx Datasheet

Enhanced 1T 8051 motor microcontrollers

Rev. 1.1.2

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1. Product Features

1.1 Features

- **Compatible with MCS-51 1T instruction set**
  - Maximum system clock frequency supports up to 48 MHz.
  - Fastest machine cycle supports $1T_{SYS}$ @ F_{SYS} ≤24MHz
  - Fastest machine cycle supports $2T_{SYS}$ @ F_{SYS}= 48MHz
- **Memory**
  - Maximum program FLASH: 16K×8Bit
  - Maximum Data FLASH: 1K×8Bit
  - Universal RAM: 256×8Bit
  - Maximum universal XRAM: 1K×8Bit
  - Program FLASH supports partition protection
- **Four oscillation modes**
  - HSI-internal RC oscillation: 24MHz/48MHz
  - HSE-external crystal oscillation: 8MHz/16MHz
  - LSE-external crystal oscillation: 32.768KHz
  - LSI-internal low power oscillation: 125KHz
- **Low voltage reset function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low voltage detection function (LVD)**
  - 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
- **GPIO**
  - Up to 16 GPIOs
  - All digital functions can be assigned to any GPIO
  - Supports pull-up/pull-down resistor function
  - Supports edge (rising/falling/both edges) interrupts
  - Supports wake-up function
- **Interrupt sources**
  - Support all external port interrupts
  - Up to 7 timer interrupts
  - Other peripheral interrupts
- **Timers**
  - WDT Timer (Watchdog Timer)
  - Up to 5 timers: Timer0/1, Timer2, Timer3/4
  - LSE Timer (Wake-up from Sleep)
  - WUT (Wake Up Timer)
  - BRT (serial port baud rate clock generator)
- **Communication modules**
  - Up to 1x SPI (communication speed up to 6Mb/s)
  - 1x I2C (communication speed up to 400Kb/s)
- **Operating voltage range**
  - 2.1V~5.5V
- **Operating temperature range**
  - -40℃~105℃
- **Buzzer**
  - 50% duty cycle: frequency can be freely set
- **Enhanced PWM**
  - Up to 6-channel enhanced PWM
  - Up to 6 independent period counters
  - Supports independent, complementary, synchronous, and group modes
  - Supports edge-aligned and center-aligned modes
  - Dead time function: supports dead time delay in complementary mode
  - Supports mask function and brake function
- **High-precision 12-bit ADC**
  - All GPIOs (16 I/Os) support AD channels
  - Reference voltage options (1.2V/2.0V/2.4V/3.0V/VDD)
  - Can detect an internal 1.2V reference voltage
  - Supports hardware-triggered boot conversion function
  - Supports a set of result digital comparison function
- **2-channel analog comparator (ACMP0/1)**
  - 5 options for positive, internal 1.2V/VDD divider available for negative
  - Comparator supports single-edge and double-edge hysteresis
  - Hysteresis voltage: 10/20/60mV
  - An EPWM brake can be triggered by the comparison outputs
  - The negative internal 1.2V/VDD divider voltage can be connected to the internal ADC channel
- **2-channel operational amplifier (OP0/1)**
  - GPIO alternate: operational amplifier ports are alternated with GPIO ports.
  - Positive: supports internal 1.2V inputs
  - Supports operational amplifier and comparator modes
  - Operational amplifier outputs can be connected to internal ADC channels
  - Operational amplifier outputs can be connected to internal analog comparator inputs

- Up to 2x UARTs (baud rate up to 1Mb/s)

- **Low power modes**
  - Idle mode (IDLE)
  - Sleep mode (STOP)
- **Supports two-wire serial programming and debugging**
  - Supports offset voltage software trimming
- **Programmable Gain Amplifier (PGA)**
  - Supports offset voltage software trimming
  - Sample-and-hold circuit (with ADC)
  - Selectable gain amplification (1/2/4/8/16/32/64/128x)
  - Supports single-ended and pseudo-differential inputs
  - PGA outputs can be connected to internal ADC channels
  - PGA outputs can be connected to internal analog comparator inputs
- **96-bit Unique ID (UID)**
  - Each chip has a distinct ID number

1.2 Product Comparison

Product model / Peripheral interface		CMS8M3510	CMS8M3512	CMS8M3524	CMS8M3536	CMS8M3536E
Internal driver supply voltage		-	8~16V	16~30V	8~20V	5~20V
Gate driver		-	3P+3N	3P+3N	6N	6N
MCU operating voltage		2.1V~5.5V				
Max. clock frequency		48 MHz				
Memory	APROM	16 KB				
	Data FLASH	1 KB				
	RAM	256 B				
	XRAM	1 KB				
Timer	WDT	1				
	Timer0/1	2 (16bit)				
	Timer2	1 (16bit)				
	Timer3/4	2 (16bit)				
	LSE Timer	1 (16bit)				
	WUT	1 (12bit)				
	BRT	1 (16bit)				
Enhanced digital peripheral	BUZZER	1				
	PWM	6(16bit)				
Comm. module	SPI	1				
	I2C	1				
	UART	2				
Analog module	12bit-ADC (channelcount)	22	15	15	16	16
	ACMP	2				
	OP	2				
	PGA	1				
GPIOs		22	15	15	16	16
LVR		1.8V/2.0V/2.5V/3.5V				
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V				
Operating voltage		2.1~5.5 V				
Operating temperature		-40~105℃				
Package		SSOP24	SSOP24	SSOP24	LQFP32	QFN32

2. System Overview

2.1 Brief Introduction

The CMS8M35xx series is an 8-bit microcontroller based on the 8051 core, compatible with the MCS-51 instruction set, featuring a 1T instruction cycle system and general-purpose I/O, with a maximum operating frequency of up to 48 MHz. The MCU has the following characteristics:

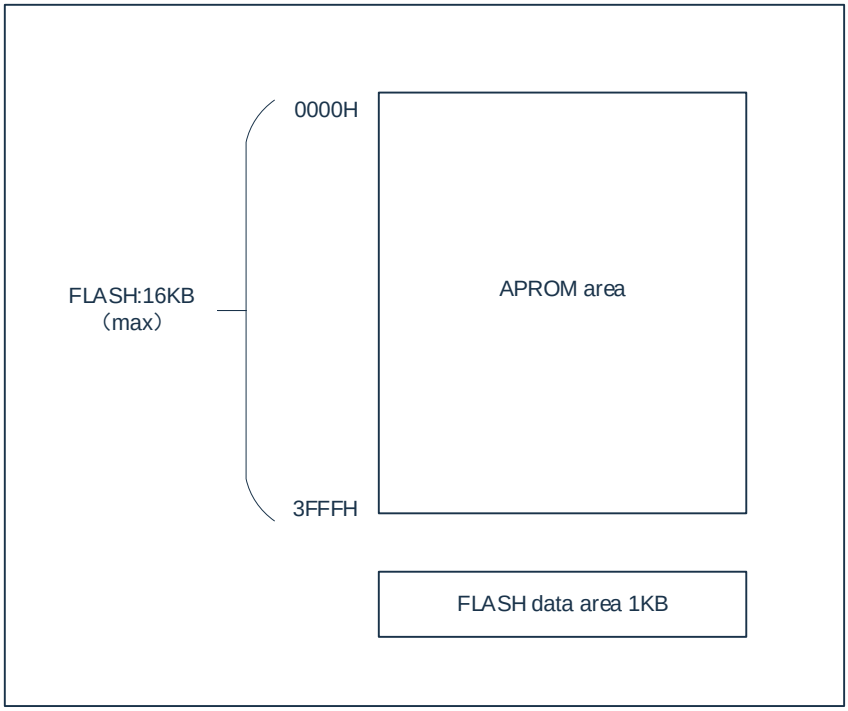
- Memory: Supports a maximum of 16KB program memory, 256B RAM, 1KB XRAM, and 1KB data memory.
- Oscillation modes: Offers four different oscillation modes.
- Power modes: Supports three operating modes: Normal, Idle Mode 1 and Sleep Mode, effectively reducing power consumption.
- Protection features: Includes low-voltage reset (LVR), low-voltage detection (LVD), and watchdog overflow reset, enhancing system reliability.
- Interrupt sources: Provides multiple interrupt sources, including external interrupts, timer interrupts, and other peripheral interrupts, enabling timely responses to external events and improving MCU utilization.
- Digital functions can be assigned to any I/O port.
- Up to nine timers capable of performing timing, counting, input capture, output comparison, timed wake-ups, and baud rate generation.
- Offers 6 channels of 16-bit PWM with support for independent, complementary, and synchronous output modes, along with hardware brake functionality, dead time control, and masked output options.
- 1 I2C module, 1 SPI module, and 2 UART modules for data transfer between the system and other devices.
- Contains a high-precision 12-bit ADC with selectable internal reference voltage, 2 operational amplifiers, 2 comparators, and 1 programmable gain amplifier, allowing each I/O to serve as an ADC input channel for enhanced analog functionality.

2.2 Memory Structure

2.2.1 Flash Memory (FLASH)

The chip has a maximum FLASH memory size of 16KB, with different product models offering varying program memory sizes depending on the specific model, with the maximum size being 16KB.

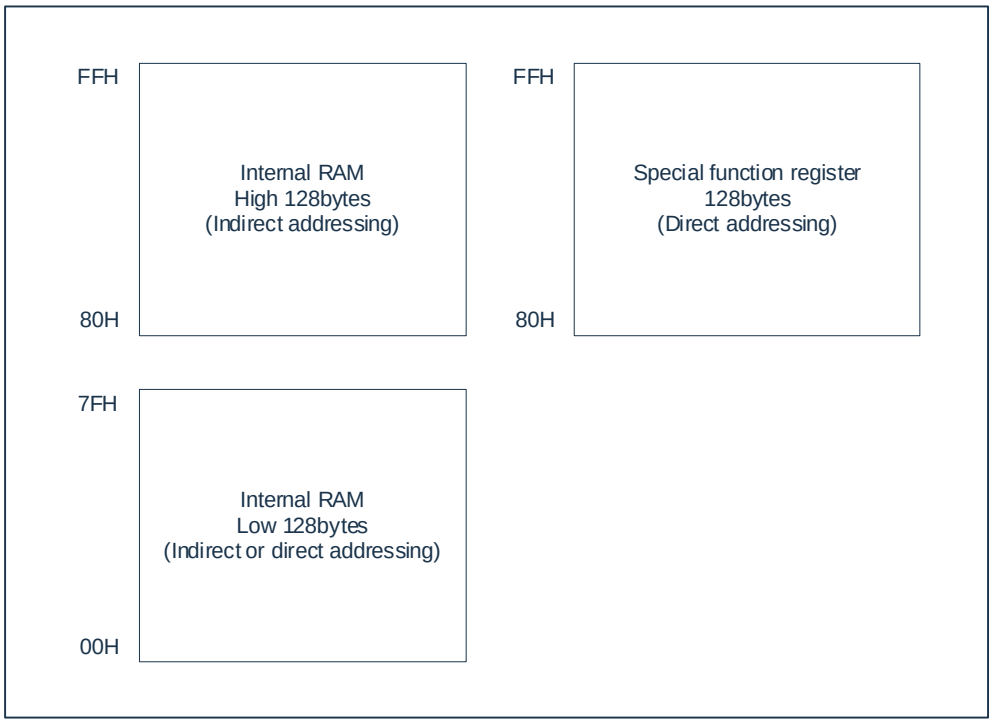
The FLASH memory allocation structure block diagram is as follows:



Address space allocation method	APROM area	
CMS8M35xx	16K	0000H-3FFFH

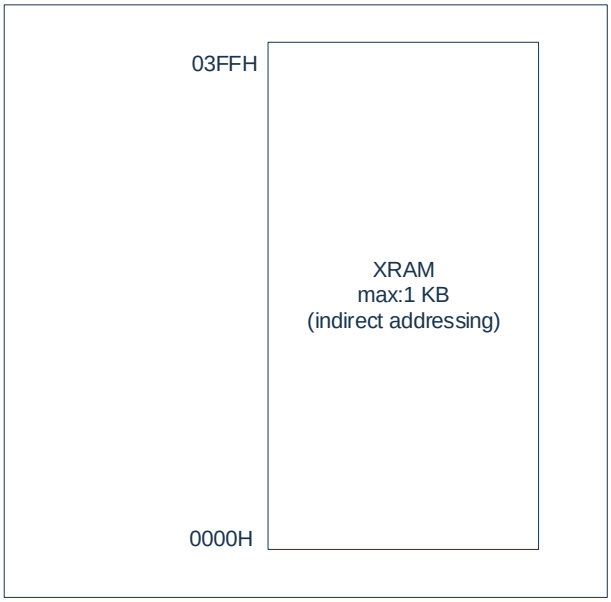
2.2.2 Internal Data Memory (RAM)

The internal data memory is divided into three parts: Low 128 Bytes, High 128 Bytes, and Special Function Registers (SFR). The RAM space allocation structure is illustrated in the diagram below:



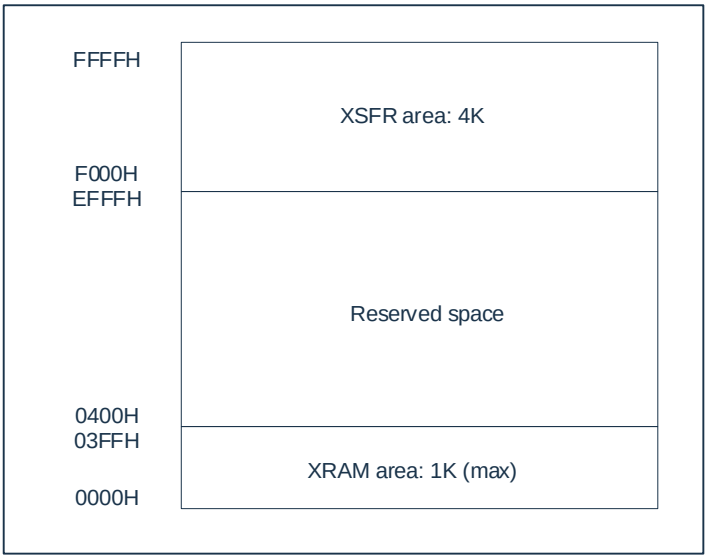
2.2.3 External Data Memory (XRAM)

The chip has a maximum of 1KB XRAM area, which is independent of the RAM/FLASH. The XRAM space allocation structure is illustrated in the diagram below:



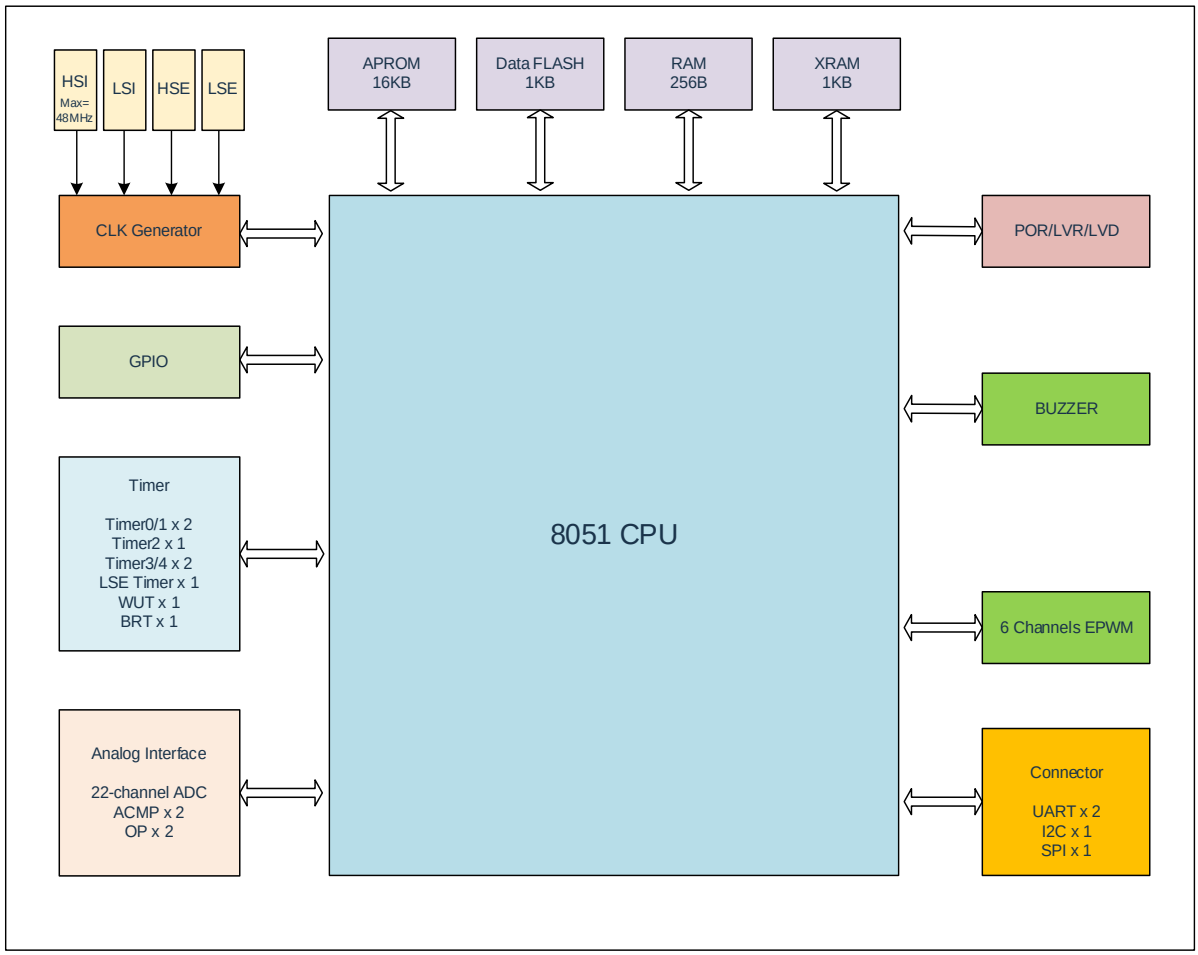
2.2.4 Special Function Register (XSFR)

The XSFR is a special register that shares the addressing space with XRAM. It primarily includes port control registers and other functional control registers. Its addressing range is as follows:

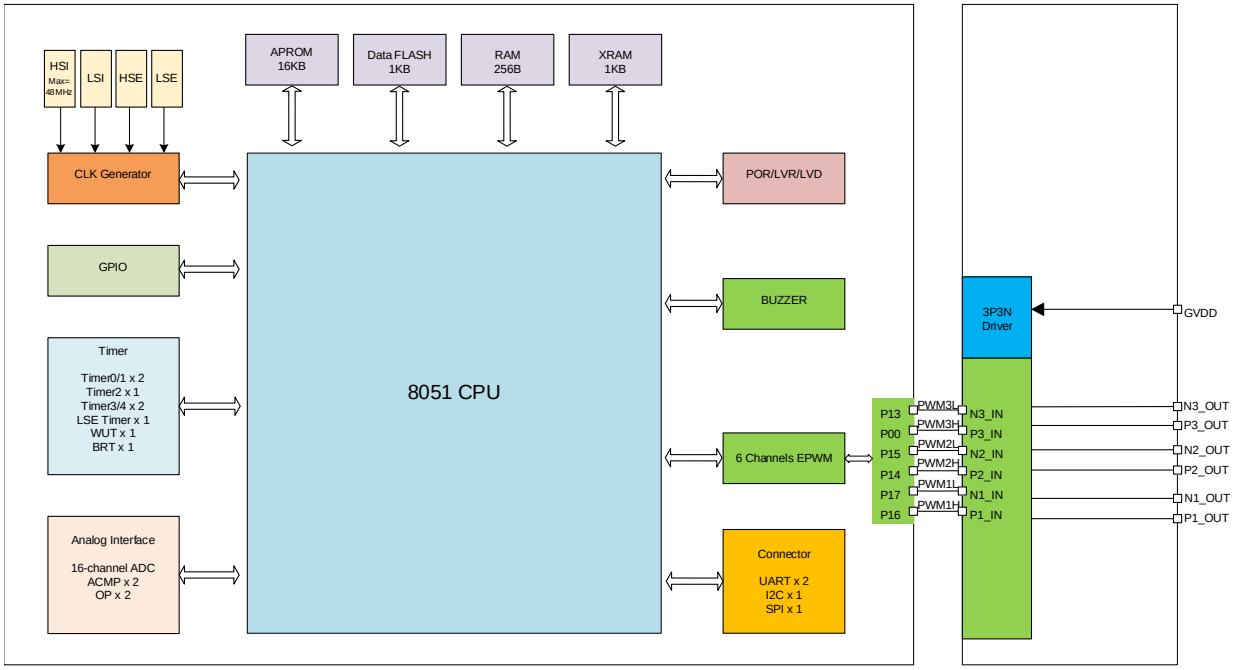


2.3 Block Diagram

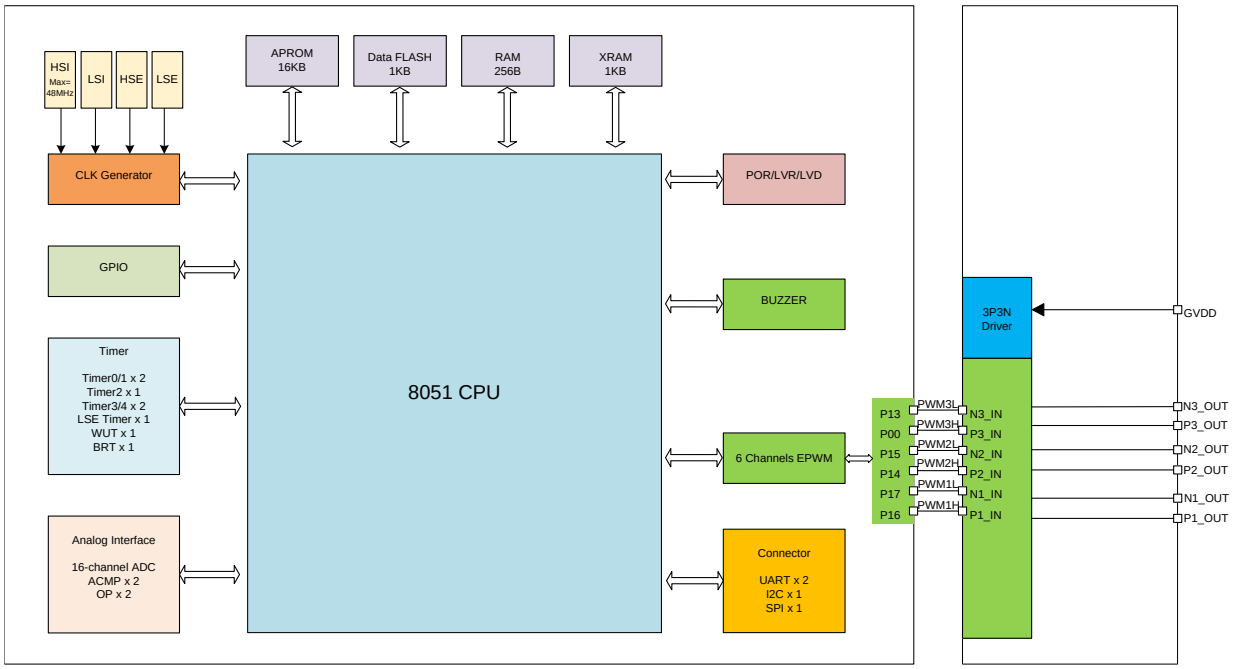
2.3.1 CMS8M3510



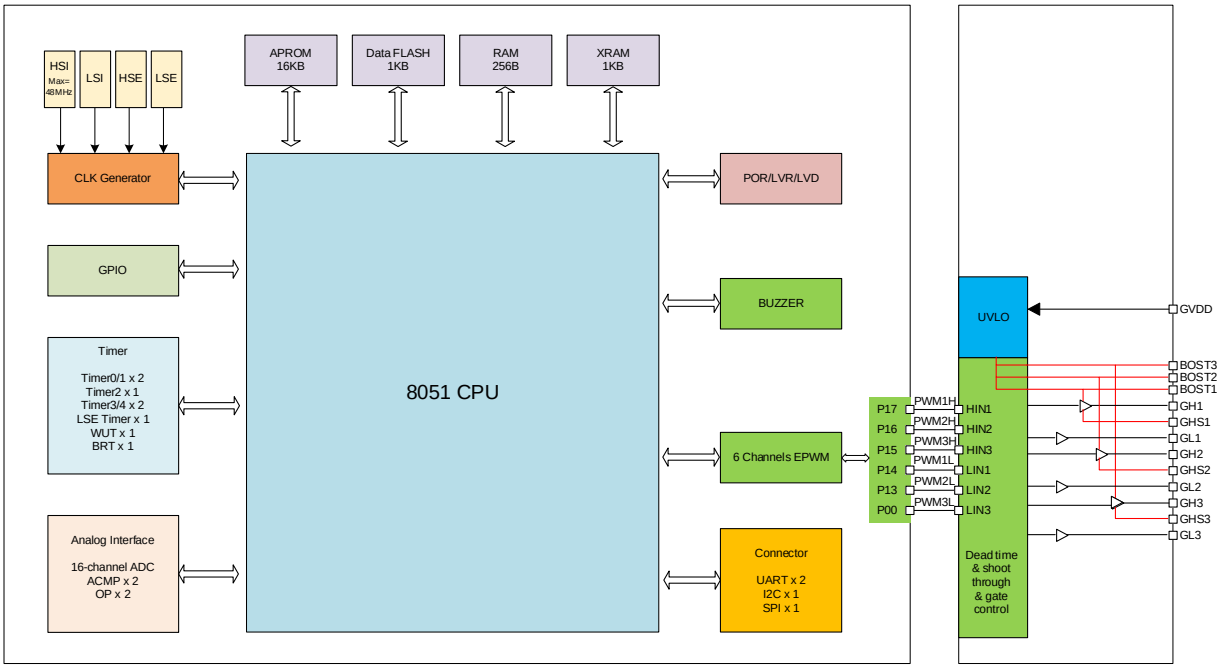
2.3.2 CMS8M3512



2.3.3 CMS8M3524



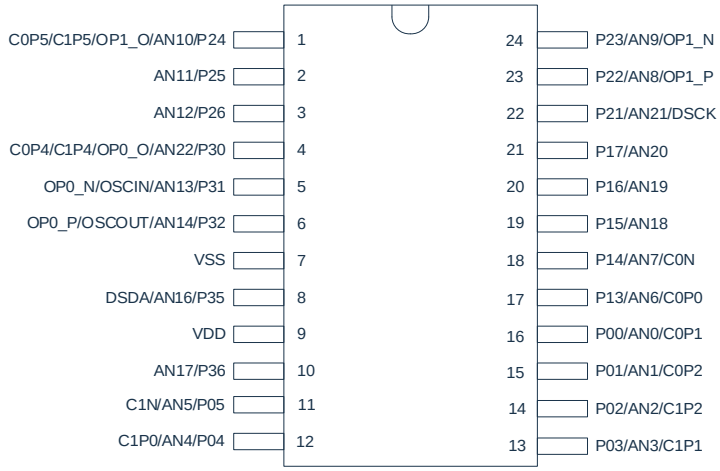
2.3.4 CMS8M3536/CMS8M3536E



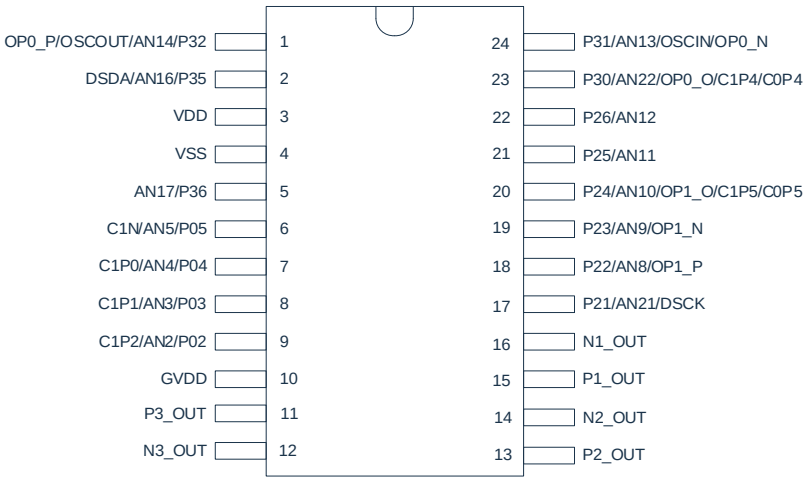
3. Pin Definition

3.1 Top View

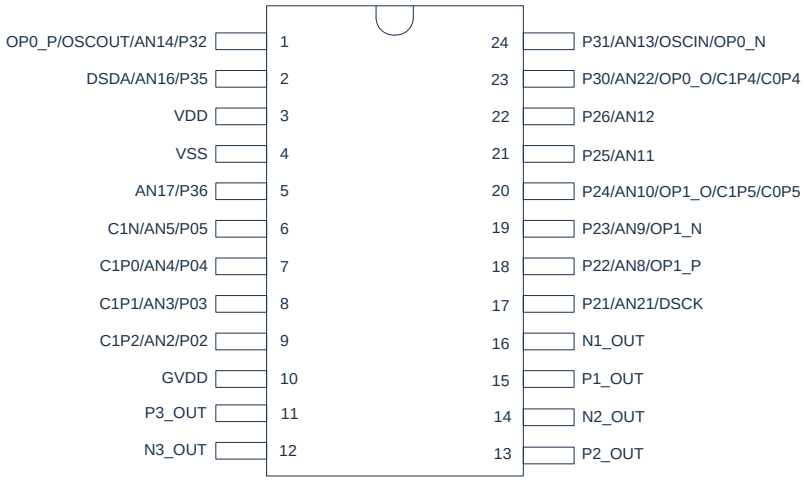
3.1.1 CMS8M3510 (SSOP24)



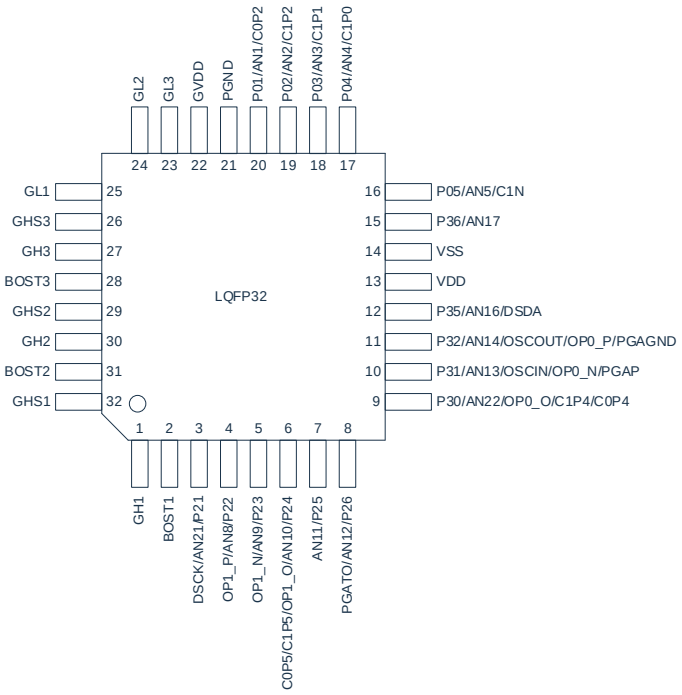
3.1.2 CMS8M3512 (SSOP24)



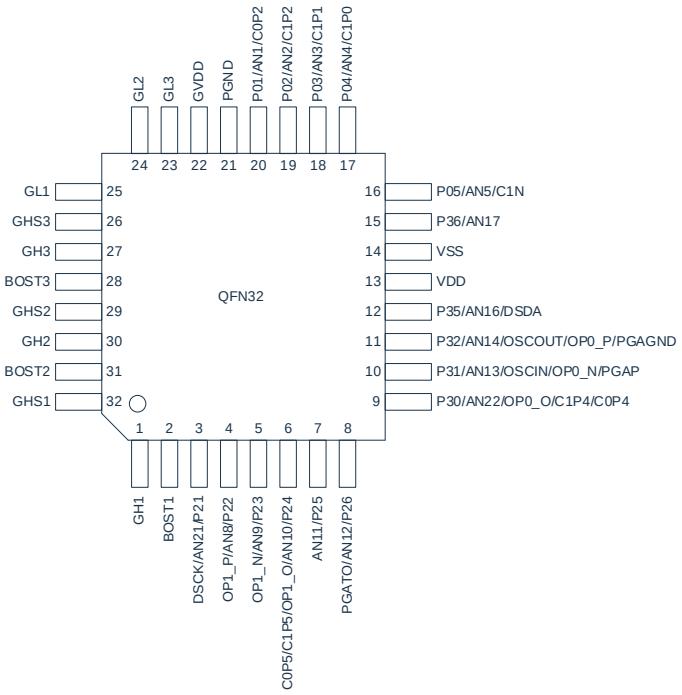
3.1.3 CMS8M3524 (SSOP24)



3.1.4 CMS8M3536 (LQFP32)



3.1.5 CMS8M3536E (QFN32)



3.2 Pin Description

Pin number				Pin name	Pin type	Description
3510	3512/ 3524	3536	3536E			
SSOP24	SSOP24	LQFP32	QFN32			
16	-	-	-	P00	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN0	ZI	ADC channel 0 input
				C0P1	AI	Comparator 0 positive channel 1 input
15	-	20	20	P01	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN1	AI	ADC channel 1 input
				C0P2	AI	Comparator 0 positive channel 2 input
14	9	19	19	P02	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN2	AI	ADC channel 2 input
				C1P2	AI	Comparator 1 positive channel 2 input
13	8	18	18	P03	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN3	AI	ADC channel 3 input
				C1P1	AI	Comparator 1 positive channel 1 input
12	7	17	17	P04	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN4	AI	ADC channel 4 input
				C1P0	AI	Comparator 1 positive channel 0 input
11	6	16	16	P05	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN5	AI	ADC channel 5 input
				C1N	AI	Comparator 1 negative channel input
17	-	-	-	P13	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN6	AI	ADC channel 6 input
				C0P0	AI	Comparator 0 positive channel 0 input
18	-	-	-	P14	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN7	AI	ADC channel 7 input
				C0N	AI	Comparator 0 negative channel input
19	-	-	-	P15	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN18	AI	ADC channel 18 input
20	-	-	-	P16	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN19	AI	ADC channel 19 input
21	-	-	-	P17	I/O	GPIO configured through registers for input,

Pin number				Pin name	Pin type	Description
3510	3512/ 3524	3536	3536E			
SSOP24	SSOP24	LQFP32	QFN32			
						output, pull-up, and pull-down functions
				AN20	AI	ADC channel 20 input
22	17	3	3	P21	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN21	AI	ADC channel 21 input
				DSCK	I/O	Programming, debugging clock input and output
23	18	4	4	P22	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN8	AI	ADC channel 8 input
				OP1_P	AI	Op-amp 1 positive input
24	19	5	5	P23	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN9	AI	ADC channel 9 input
				OP1_N	AI	Op-amp 1 negative input
1	20	6	6	P24	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN10	AI	ADC channel 10 input
				C0P5	AI	Comparator 0 positive channel 5 input
				C1P5	AI	Comparator 1positive channel 5 input
				OP1_O	AO	Op-amp 1 output
2	21	7	7	P25	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN11	AI	ADC channel 11 input
3	22	8	8	P26	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN12	I	ADC channel 12 input
				PGATO	AO	PGA test output
4	23	9	9	P30	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN22	AI	ADC channel 22 input
				C0P4	AI	Comparator 0 positive channel 4 input
				C1P4	AI	Comparator 1 positive channel 4 input
				OP0_O	AO	Op-amp 0 output
5	24	10	10	P31	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN13	AI	ADC channel 13 input
				OSCIN	AI	External oscillator input

Pin number				Pin name	Pin type	Description
3510	3512/ 3524	3536	3536E			
SSOP24	SSOP24	LQFP32	QFN32			
				OP0_N	AI	Op-amp 0 negative input
				PGAP	AI	PGA positive input
6	1	11	11	P32	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN14	AI	ADC channel 14 input
				OSCOUT	O	External oscillator output
				OP0_P	AI	Op-amp 0 positive input
				PGAGND	AI	PGA feedback ground input
8	2	12	12	P35	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN16	AI	ADC channel 16 input
				DSDA	I/O	Programming, debugging data input and output
10	5	15	15	P36	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
				AN17	AI	ADC channel 17 input
9	3	13	13	VDD	P	Power supply voltage input pin
7	4	14	14	VSS	P	Ground pin
-	-	21	21	PGND	P	Internal pre-driver ground pin
	10	22	22	GVDD	P	Internal pre-driver power pin
-	-	23	23	GL3	O	Phase 3 low-side gate drive output pin
-	-	24	24	GL2	O	Phase 2 low-side gate drive output pin
-	-	25	25	GL1	O	Phase 1 low-side gate drive output pin
-	-	26	26	GHS3	P	Phase 3 high-side floating ground pin
-	-	27	27	GH3	O	Phase 3 high-side gate drive output pin
-	-	28	28	BOST3	P	Phase 3 high-side bootstrap supply pin
-	-	29	29	GHS2	P	Phase 2 high-side floating ground pin
-	-	30	30	GH2	O	Phase 2 high-side gate drive output pin
-	-	31	31	BOST2	P	Phase 2 high-side bootstrap supply pin
-	-	32	32	GHS1	P	Phase 1 high-side floating ground pin
-	-	1	1	GH1	O	Phase 1 high-side gate drive output pin
-	-	2	2	BOST1	P	Phase 1 high-side bootstrap supply pin
-	11	-	-	P3_OUT	O	Phase 3 PMOS driver pin
-	12	-	-	N3_OUT	O	Phase 3 NMOS driver pin
-	13	-	-	P2_OUT	O	Phase 2 PMOS driver pin
-	14	-	-	N2_OUT	O	Phase 2 NMOS driver pin
-	15	-	-	P1_OUT	O	Phase 1 PMOS driver pin
-	16	-	-	N1_OUT	O	Phase 1 NMOS driver pin

3.3 GPIO Features

The GPIO pins support multiple shared functions, with each I/O port configurable for any digital function or specified analog function. As general-purpose GPIO ports, they have the following features:

- Configurable for two output speed levels.
- Configurable for two drive current levels.
- Able to read the status of data latches or pin states.
- Configurable for interrupt triggering on rising edge, falling edge, or both edges.
- Configurable for interrupt wake-up on rising edge, falling edge, or both edges.
- Configurable as normal input, pull-up input, pull-down input, push-pull output, or open-drain output mode.

3.4 Pin Function List

The digital functions of the pins on the CMS8M35xx series chip can be freely assigned, meaning each I/O pin can be assigned any digital function. The assignable digital functions are shown in the table below:

Digital function	Direction	Function description
GPIO	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
CC0	O	Timer2 compare output channel 0
CC1	O	Timer2 compare output channel 1
CC2	O	Timer2 compare output channel 2
CC3	O	Timer2 compare output channel 3
TXD0	O	UART0 data output
RXD0	I/O	UART0 data input/synchronous mode data output
TXD1	O	UART1 data output
RXD1	I/O	UART1 data input/synchronous mode data output
SCL	I/O	I^2C clock input/output
SDA	I/O	I^2C data input/output
NSS	I/O	SPI slave mode chip select signal (input/output)
SCLK	I/O	SPI clock input/output
MOSI	I/O	SPI master transmit/slave receive
MISO	I/O	SPI master receive/slave transmit
PG0	O	PWM channel 0 output
PG1	O	PWM channel 1output
PG2	O	PWM channel 2 output
PG3	O	PWM channel 3 output
PG4	O	PWM channel 4 output
PG5	O	PWM channel 5 output
BEEP	O	Buzzer drive output
C0_O	O	Comparator 0 output
C1_O	O	Comparator 1 output
INT0	I	External interrupt 0 input
INT1	I	External interrupt 1 input
T0	I	Timer0 external clock input
T0G	I	Timer0 gate input
T1	I	Timer1 external clock input
T1G	I	Timer1 gate input
T2	I	Timer2 external event or gate input
T2EX	I	Timer2 falling edge auto reload input
CAP0	I	Timer2 input capture channel 0
CAP1	I	Timer2 input capture channel 1
CAP2	I	Timer2 input capture channel 2
CAP3	I	Timer2 input capture channel 3

Digital function	Direction	Function description
ADET	I	ADC external trigger input
FB	I	PWM external brake signal input

The allocation of analog functions for the pins is fixed, with each pin assigned a different analog function. The actual pin assignments are based on the specific product. The allocation of analog functions is shown in the table below:

PIN	CONFIG	1(ANALOG)				Other digital function priority
P0.0	-	AN0	C0P1	-	-	Highest
P0.1	-	AN1	C0P2	-	-	
P0.2	-	AN2	C1P2	-	-	
P0.3	-	AN3	C1P1	-	-	
P0.4	-	AN4	C1P0	-	-	
P0.5	-	AN5	C1N	-	-	
P1.3	-	AN6	C0P0	-	-	
P1.4	-	AN7	C0N	-	-	
P1.5	-	AN18	-	-	-	
P1.6	-	AN19	-	-	-	
P1.7	-	AN20	-	-	-	
P2.1	DSCK	AN21	-	-	-	
P2.2	-	AN8	-	OP1_P	-	
P2.3	-	AN9	-	OP1_N	-	
P2.4	-	AN10	C0P5/C1P5	OP1_O	-	
P2.5	-	AN11	-	-	-	
P2.6	-	AN12	-	-	PGATO	
P3.0	-	AN22	C0P4/C1P4	OP0_O	-	
P3.1	OSCIN	AN13	-	OP0_N	PGAP	
P3.2	OSCOUT	AN14	-	OP0_P	PGAGND	
P3.5	DSDA	AN16	-	-	-	
P3.6	-	AN17	-	-	-	Lowest

4. Function Summary

4.1 System Clock

The system clock is controlled through the settings of the system configuration register and the oscillator control register, allowing for clock source and clock division selection. The chip clock source can be selected from the following four types:

- Internal high-speed oscillator (HSI) (24MHz/48MHz).
- External high-speed oscillator (HSE) (8 MHz/16 MHz).
- External low-speed oscillator (LSE) (32.768 kHz).
- Internal low-speed oscillator (LSI) (125 kHz).

4.2 Reset

Reset operations are used to initialize the internal circuits of the chip, allowing the system to start from a defined state. The chip has the following types of reset:

- Power-on reset.
- External reset.
- Low voltage reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.
- Watchdog overflow reset.
- Software reset.

Any of the above reset situations require a certain response time, and the system provides a comprehensive reset process to ensure the smooth execution of the reset actions.

4.3 Power Management

4.3.1 Operating Mode

The chip has three different operating modes to accommodate various power consumption needs for different applications:

- Normal mode: The MCU operates in normal mode, with peripherals functioning as expected.
- Idle mode (IDLE): In this mode, the MCU is in Idle Mode, where the CPU stops working, but the peripherals continue to operate. This mode can be awakened by any interrupt.
- Sleep mode (STOP): In sleep mode (STOP), the MCU halts all operations, with peripherals turned off. This mode can be awakened by INT0/1 interrupt, external interrupts, WUT timer wake-up, or LSE timer wake-up.

4.3.2 Low Voltage Reset (LVR)

When the power supply voltage falls below the set detection voltage, the system will reset.

There are four options for the low voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Low Voltage Detection (LVD)

This series of products contains a low-voltage detection circuit that can compare the power supply voltage with the set detection voltage. If the power supply voltage is lower than the set detection voltage, an interrupt request signal is generated.

There are 8 options for detection voltage: 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V.

4.4 Interrupt Control

The chip features multiple interrupt sources and interrupt vectors. User-configurable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, PWM, I2C, SPI, UART0/1, P0/P1/P2/P3, ACMP0/1, ADC, and LVD. The actual number of interrupt sources may vary by product.

The chip supports two interrupt priority levels, allowing for two-level interrupt nesting. If an interrupt is currently being serviced and a higher-priority interrupt request occurs, the latter can interrupt the former, enabling nested interrupts.

4.5 Timers

4.5.1 WDT

The Watchdog Timer (WDT) is an on-chip timer that uses the system clock as its time source. A WDT overflow will trigger a reset. The watchdog reset serves as a protective mechanism for the system, allowing it to reset in case it enters an unknown state, thus preventing it from getting stuck in an infinite loop. The WDT timer has the following features:

- Eight selectable WDT overflow timing levels.
- Configurable watchdog overflow interrupt.
- Configurable watchdog overflow reset.

4.5.2 Timer0/1

Timer 0 and Timer 1 share similar types and structures, both functioning as 16-bit up-counting timers. Timer 0 offers four operational modes, while Timer 1 provides three, enabling basic timing and event counting operations.

In timer mode, the timer register increments every 12 or 4 system cycles when the timer clock is enabled. In counter mode, the timer register increments upon detecting a falling edge on the corresponding input pins (T0 or T1). Timer 0/1 has the following features:

- Can be used as a normal timer.
- Supports gated timing functionality.
- Supports external counting functionality.
- Supports gated counting functionality.
- Generates counter overflow interrupts.

4.5.3 Timer2

Timer 2 is a 16-bit timer designed for generating various digital signals and event capturing, such as pulse generation, pulse width modulation, and pulse width measurement. Timer 2 has the following features:

- Can be used as a normal timer.
- Supports gated timing functionality.
- Supports external counting functionality.
- Includes reload-disable, automatic overflow reload, and automatic reload on external pin falling edge.
- Can trigger capture on rising edge, falling edge, both edges, or writing to the low byte of the capture register.
- Features a comparison function that can generate periodic signals with controllable duty cycle PWM waveforms.
- Supports interrupts for timing, external triggers, capture, and comparison operations.

4.5.4 Timer3/4

Timer 3 and Timer 4 are similar to Timer 0 and Timer 1, functioning as two 16-bit timers. Timer 3 has four operating modes, while Timer 4 has three operating modes. Unlike Timer 0 and Timer 1, Timer 3 and Timer 4 only provide timer operations.

When the timers are started, the values in the registers (counters) increment once every 12 or 4 system cycles.

4.5.5 LSE Timer

The LSE timer is a 16-bit up-counting timer with a clock source derived from an external low-speed clock (LSE). The LSE timer has the following features:

- Timing functionality.
- Supports setting a 16-bit timing value.
- Can operate normally in sleep mode.
- Generates an interrupt when the count value equals the timing value.
- Timing interrupts can wake the device from idle mode/sleep mode.

4.5.6 WUT

The WUT (Wake-Up Timer) is a 12-bit up-counting timer with a clock source derived from the internal low-speed clock (LSI), designed for waking the system from sleep mode. After the system enters sleep mode, the CPU and all peripheral circuits stop working, while the internal low-speed clock LSI provides the clock for the WUT counter. The WUT has the following features:

- Can wake the system from sleep state.
- Count clock can be configured with division factors of 1, 8, 32, or 256.
- Supports setting a 12-bit timing value.

4.5.7 BRT

The BRT (Baud Rate Timer) is a 16-bit timer with a clock source derived from the system clock, primarily providing clock signals for the UART module. The BRT has the following features:

- Independent control switch.
- Count clock with 8 selectable division factors.
- 16-bit incremental counting.

4.6 Enhanced Digital Peripherals

4.6.1 Buzzer

The buzzer driver consists of an 8-bit counter, a clock driver, and a control register, generating a square wave with a 50% duty cycle and a broad frequency range. The BUZZER has the following features:

- Independent enable control switch.
- Selectable system clock division ratios of 8, 16, 32, and 64.
- Output frequency controlled by an 8-bit value, adjustable from (1 to 255) x 2 division output.

4.6.2 Enhanced PWM Module

The enhanced PWM module supports six PWM generators, with independent configuration for period and duty cycle. The PWM module features:

- Supports two waveform output modes: one-shot and continuous.
- Supports four control modes: independent, complementary, synchronous, and group control.
- Selectable counting clock division factors of 1, 2, 4, 8, and 16.
- Supports two counting modes: edge-aligned and center-aligned, with symmetric and asymmetric counting in center-aligned mode.
- Supports mask output.
- Supports dead time programming.
- Configurable output polarity.
- Supports period, up-count comparison, down-count comparison, and zero-point interrupts.
- Supports software brake, external port trigger brake, ADC comparison result trigger brake, and ACMP output trigger brake.

4.7 Communication Modules

4.7.1 SPI Module

The SPI (Serial Peripheral Interface) is a fully configurable master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI enables communication between the MCU and serial peripheral devices, and it can also facilitate inter-processor communication in multi-master systems. The SPI features include:

- Full-duplex synchronous serial data transmission.
- Supports master/slave modes.
- Supports multi-master systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock ($F_{SYS} \leqslant 24MHz$).
- Bit rates generated at 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, and 1/512 of the system clock.
- Supports four transmission formats.
- Interrupt generation upon completion of transmit/receive operations.

4.7.2 I²C Module

The I²C module is a two-wire bidirectional serial bus controller that provides a simple and efficient means for data exchange between microprocessors and I²C buses. The I²C module features include:

- Supports four operating modes: master transmit, master receive, slave transmit, and slave receive.
- Supports two transmission speed modes:
  Standard mode (up to 100 Kb/s)
  Fast mode (up to 400 Kb/s)
- Handles arbitration and clock synchronization.
- Supports multi-master systems.
- Master mode supports 7-bit and 10-bit addressing modes on the I²C bus (software supported).
- Slave mode supports 7-bit addressing on the I²C bus.
- Allows operation over a wide clock frequency range (with built-in 8-bit timer).
- Interrupt generation upon completion of receive/transmit operations.

4.7.3 UARTn Module

The UARTn module includes UART0 and UART1. The UARTn features include:

- Full-duplex serial port.
- Supports synchronous mode.
- Supports variable baud rate in 8-bit asynchronous transmission mode.
- Supports variable baud rate in 9-bit asynchronous transmission mode.
- Baud rate can be generated by Timer1, Timer4, Timer2, or the BRT module.
- Interrupt generation upon completion of transmit/receive operations.

4.8 Analog Modules

4.8.1 Analog-to-Digital Converter (ADC)

The ADC module is a 12-bit successive approximation analog-to-digital converter. The port's analog input signals are connected to the ADC input through a multiplexer, and the ADC generates a 12-bit binary result based on the input analog signal, storing this result in the ADC result register. The ADC features include:

- All I/O ports can serve as external input channels for the ADC.
- 8 selectable clock frequencies for ADC conversion.
- ADC reference voltage options: VDD/1.2V/2.0V/2.4V/3.0V.
- A complete 12-bit conversion requires 18.5 ADC conversion cycles.
- Supports external port edge and enhanced PWM trigger for ADC conversion.
- Supports ADC conversion result comparison output, which can control enhanced PWM brake function.
- Supports interrupt generation upon ADC conversion completion.

4.8.2 Analog Comparators (ACMP0/1)

The comparators ACMP0 and ACMP1 feature the following characteristics:

- Positive input supports multiple selectable input ports.
- Negative input can be selected from port input or internal reference voltage.
- Internal reference voltage divider has 16 selectable levels.
- Supports output filtering with 11 selectable filter time options.
- Supports single-side and double-side hysteresis control.
- Hysteresis voltage options: 10mV, 20mV, or 60mV.
- Supports software trimming for offset voltage.
- Output can serve as a braking trigger signal for enhanced PWM.
- Supports interrupt generation upon output change.

4.8.3 Operational Amplifiers (OP0/1)

The operational amplifiers (OP0 and OP1) feature the following characteristics:

- Positive input supports internal 1.2V voltage.
- Supports both comparator and operational amplifier modes.
- Output can be connected to the internal ACMP input for shaping.
- Output can also be connected to ADC channel 31 for measurement.
- Supports software trimming for offset voltage.

4.8.4 Programmable Gain Amplifier (PGA)

The programmable gain amplifier (PGA) features the following characteristics:

- Multiple selectable gains (1/2/4/8/16/32/64/128).
- PGA input with a sample-and-hold circuit.
- Supports single-ended and pseudo-differential inputs.
- Supports PGA output testing.
- PGA output can be connected to the internal analog comparator input for shaping.
- PGA output can be internally connected to ADC internal channel 31 for measurement.
- Supports software trimming for offset voltage.

4.9 FLASH Memory

The FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH). Access operations can be performed through related Special Function Registers (SFR) to enable In-Application Programming (IAP) functionality. FLASH memory supports the following operations:

- Byte read operations.
- Byte write operations.
- Page erase operations.

4.10 Unique ID (UID)

Each chip has a 96-bit unique identification number, known as the Unique ID (UID). The UID is set at the factory and cannot be modified by the user.

5. User Configuration

The System Configuration Register (CONFIG) contains the FLASH options for the MCU's initial conditions and cannot be accessed or modified by the program. The following settings can be configured through the System Configuration Register:

- Watchdog operating mode.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset threshold.
- Debug mode enable or disable.
- Oscillation mode and prescaler selection.
- Internal high-speed oscillator divider selection.
- External reset configuration and port selection.
- Sleep wake-up wait time.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	V_{DD} maximum input current	-	120	mA
I_{SS}	V_{SS} maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single I/O	-	50	mA
	Maximum source current of a single I/O	-	20	mA
	Maximum sink current of all I/Os	-	120	mA
	Maximum source current of all I/Os	-	120	mA

Caution: Permanent damage to the MCU may result if **absolute maximum ratings** are exceeded. Functionality is guaranteed only when the device operates within the specified range in the manual. Operating the chip under absolute maximum ratings conditions may affect the device's reliability.

6.2 DC Electrical Parameters

VDD-VSS=2.1~5.5V, T_A=25℃

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Operating voltage	F_{SYS}=48MHz, F_{CPU}=F_{SYS}/2 F_{SYS}=8MHz~24MHz, F_{CPU}=F_{SYS}	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	6	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	6	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals off F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals off F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals off F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals off F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off F_{CPU}=F_{SYS}	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals off F_{CPU}=F_{SYS}	-	2	-	mA
	IDLE mode	VDD=5V, F_{SYS}=48MHz, all peripherals off	-	4	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off	-	4	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals off	-	2.5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals off	-	2.5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals off	-	2	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals off	-	2	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off	-	1.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals off	-	1.5	-	mA
I_{SLEEP1}	Sleep current	All peripherals off, LSE, LSE timer enabled	-	20	-	uA
I_{SLEEP2}	Sleep current	All peripherals off, LSI, WUT timer enabled	-	7	-	uA
I_{SLEEP3}	Sleep current	All peripherals off	-	6	-	uA
I_{LI}	Input leakage current	-	-	-	0.1	uA
V_{IL}	Input level, low	-	VSS	-	0.3VDD	V
V_{IH}	Input level, high	-	0.7VDD	-	VDD	V
V_{OL}	Output voltage, low	VDD=5V, I_{OL1}=12mA	-	-	0.4	V
		VDD=5V, I_{OL2}=7mA	-	-	0.4	V
		VDD=3V, I_{OL1}=9mA	-	-	0.4	V
		VDD=3V, I_{OL2}=5mA	-	-	0.4	V
V_{OH}	Output voltage, high	VDD=5V, I_{OH1}=40mA	3.5	-	-	V
		VDD=5V, I_{OH2}=20mA	3.5	-	-	V
		VDD=3V, I_{OH1}=15mA	2.1	-	-	V
		VDD=3V, I_{OH2}=8mA	2.1	-	-	V
R_{PH}	Pull-up resistance	-	-	32	-	KΩ
R_{PL}	Pull-down resistance	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-On Reset Time

T_A=25℃, excluding the reset time of the 32.768K crystal oscillator.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	μs/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	μs/V

6.3.2 External Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

Symbol	Parameter	Test condition	Frequency error	Min.	Typ.	Max.	Unit
F_{HSI}	Internal high-speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low-speed 125KHz	T_A=25℃	±5%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

6.3.4 Low-Voltage Reset Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low voltage detection threshold value: 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low voltage detection threshold value: 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low voltage detection threshold value: 3.5V	3.35	3.5	3.65	V

6.3.5 LVD Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVD1}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low voltage detection threshold value: 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low voltage detection threshold value: 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low voltage detection threshold value: 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low voltage detection threshold value: 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low voltage detection threshold value: 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low voltage detection threshold value: 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low voltage detection threshold value: 4.3V	4.15	4.3	4.45	V

6.4 Flash Electrical Parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	27	105	℃
$N_{ENDURANCE}$	Erase count	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erasing time	-	-	1.5	-	ms
T_{PROG}	Programming time	-	-	7	-	μs
I_{DD1}	Reading time	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erasing current	-	-	-	2	mA

6.5 Analog Circuit Characteristics

6.5.1 BANDGAP Electrical Characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal reference 1.2V	VDD=2.1~5.5V, T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V, T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V, T_A=-40℃ to 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (Note1, Note2) (Non-V_{BG})		1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3 (Note2)		1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4 (Note 2)		2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5 (Note 2)		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	Resolution		12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5μs)		±2			LSB
INL	Integral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5μs)		±4			LSB
T_{ADCK}	ADC clock period	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF}=V_{REF2}	32	-	-	us
		V_{REF} =V_{REF3}/ V_{REF4}/V_{REF5}	2	-	-	us
T_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)		100			Ksps

Note 1: When V_{REF} =V_{REF2}, the accuracy is 8-bit.

Note 2: Test condition: T_A=25°C, V_{AVDD}=5.0V.

6.5.3 ACMP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Before zeroing	-	±4.0	-	mV
		After zeroing	-	±0.5	±1.0	
V_{CM}	Common mode input voltage range	-40℃~105℃	-0.1	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input offset voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	150	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃~105℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stable time	-	-	-	5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

6.5.4 OP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, VIN+=1V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0mV	-	1.0	1.6	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Before zeroing	-	±3.5	-	mV
		After zeroing	-	±0.5	±1.0	
V_{CM}	Common mode input voltage range	-40℃~105℃	0	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.3	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	R_{LOAD}=2K, C_{LOAD}=100pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	75	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~ (VDD-1.5) -40℃~105℃	-	90	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD} =2K, C_{LOAD} =100pF	-	±8	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

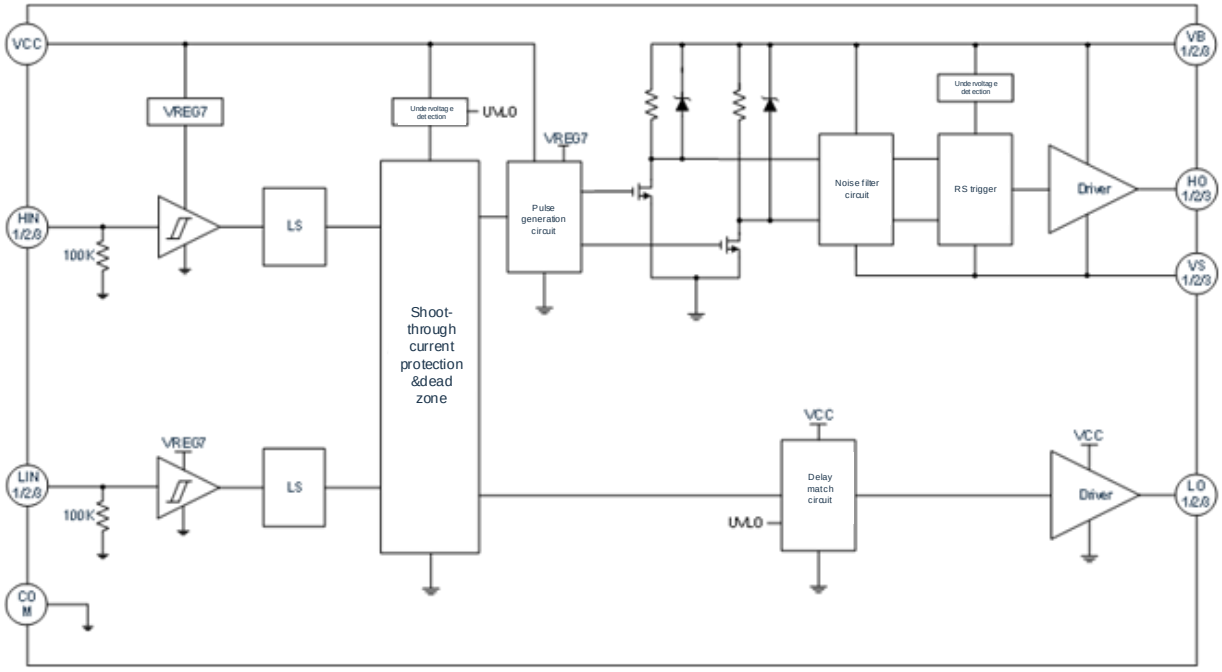
6.5.5 PGA Eectrical Characteristics

T_A=25℃, VDD=5V, V_{IN+}=0.01V, unless otherwise specified (G is the gain factor).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.5	0.7	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Before zeroing	-	±2.5	-	mV
		After zeroing	-	±0.1	±0.2	
V_{CM}	Common mode input voltage range	G=1	0.032	-	(VDD-1.5)/G	V
		G=2	0.016			
		G=4	0.008			
		G=8	0.004			
		G=16	0.002			
		G=32, 64,128	0.001			
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=1, 2, 4, 8, 16	-1	-	1	%
		G=32	-2	-	2	
		G=64,128	-4	-	4	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-1.5	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.032	-	-	V
Frequency characteristics						
BW	Bandwidth	C_{LOAD}=10pF, G=1	-	1.5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, G=16	-	75	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF, G=32	-	10	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs
$T_{SH(1)}$	Sample hold time	-	-	3	-	μs

6.6 Gate Driver (6N) Electrical Characteristics (CMS8M3536)

6.6.1 Internal Logic Block Diagram



6N pre-driver internal logic block diagram

6.6.2 Absolute Maximum Ratings

(T_A=25°C, unless otherwise specified, all pins are referenced to GND.)

Parameter	Symbol	Min.	Max.	Unit
High-side floating offset absolute voltage	$VB_{1,2,3}$	-0.3	225	V
High-side floating offset relative voltage	$V_{S1,2,3}$	$V_{B1,2,3}$-25	$V_{B1,2,3}$+0.3	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3	$V_{B1,2,3}$+0.3	V
Maximum supply voltage	VCC	-0.3	25	V
Low-side output voltage	$V_{LO1,2,3}$	-0.3	VCC	V
Maximum input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	-0.3	10	V
Maximum offset voltage slew rate	dVS/dt	-	50	V/ns
Thermal resistance junction-to-ambient	θ_{JA}	-	54	°C/W
Junction temperature	I_J	-	150	°C
Storage temperature	I_S	-55	150	°C
Pin soldering temperature (duration 10s)	I_L	-	260	°C
ESD (Note2)	V_{ESD}	-	2000	V

Note:

1) T_A is the operating temperature at which the circuit operates, θ_{JA} is the thermal resistance of the package, 150°C is the maximum operating junction temperature of the circuit.
2) For the Human Body Model (HBM), a 100pF capacitor discharges through a 1.5kΩ resistor.
3) If the operating conditions of the circuit exceed the absolute maximum ratings, it is very likely that the circuit will be damaged immediately.

6.6.3 Recommended Operating Conditions

(T_A=25°C, unless otherwise specified, all pins are referenced to GND.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-side floating offset absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+8	$V_{S1,2,3}$+15	$V_{S1,2,3}$+20	V
High-side floating offset relative voltage	$V_{S1,2,3}$	GND-5	-	200	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{S1,2,3}$+15	$V_{B1,2,3}$	V
Supply voltage	VCC	8	15	20	V
Low-side output voltage	$V_{LO1,2,3}$	0	15	VCC	V
Input voltage (HIN1,2,3 /LIN1,2,3)	V_{IN}	0	-	5	V

Note: T_A is the operating temperature at which the circuit operates.

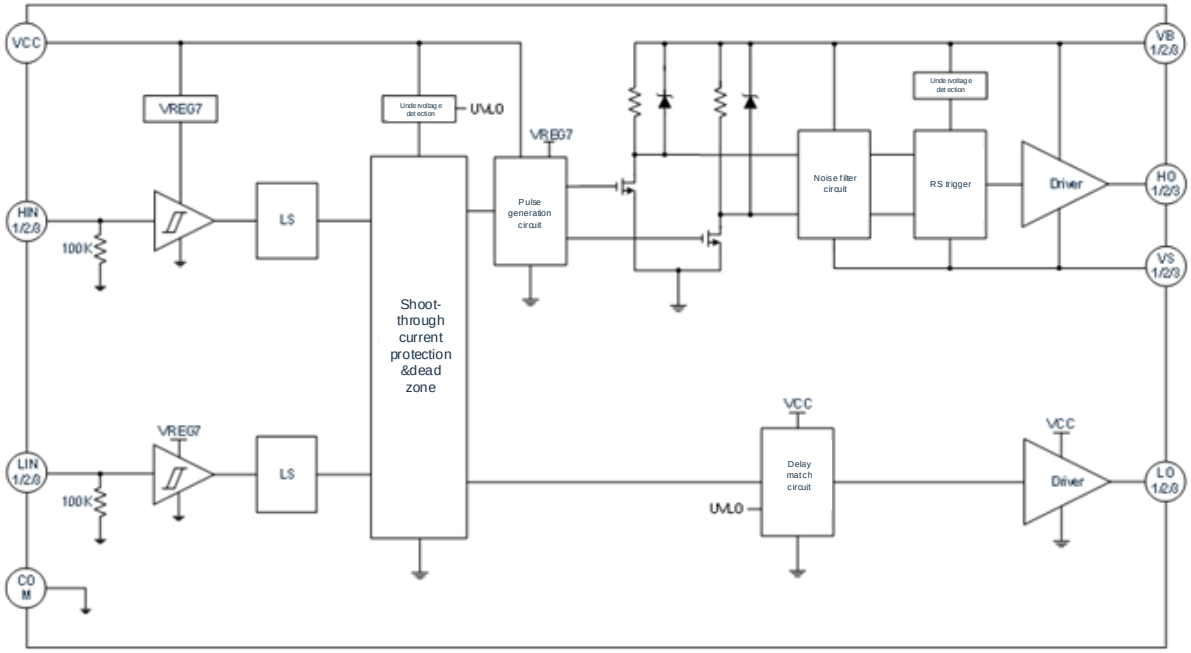
6.6.4 Table of Electrical Characteristics

(T_A=25℃, V_{CC}=$V_{BS1,2,3}$=15V, $V_{s1,2,3}$=GND, all pins are referenced to GND unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power current parameters						
V_{CC} quiescent current	I_{CCQ}	V_{IN}=0V	225	330	460	μA
V_{BS} quiescent current	I_{BSQ}	V_{HIN}=0V	30	54	70	μA
V_{CC} dynamic current	I_{CCD}	$f_{LIN1,2,3}$=20KHz	300	560	750	μA
V_{BS} dynamic current	I_{BSD}	$f_{HIN1,2,3}$=20KHz	120	180	240	μA
V_B floating power leakage current	I_{LK}	V_B=225V	-	-	0.1	μA
Power supply voltage parameters						
V_{CC} undervoltage high-level voltage	V_{CCHY+}		5.5	6.8	7.0	V
V_{CC} undervoltage low-level voltage	V_{CCHY-}		5.0	6.2	6.5	V
V_{CC} undervoltage hysteresis voltage	V_{CCHY}		-	0.6	-	V
V_{BS} undervoltage high-level voltage	V_{BSHY+}		5.5	6.8	7.0	V
V_{BS} undervoltage low-level voltage	V_{BSHY-}		5.0	6.2	6.5	V
V_{BS} undervoltage hysteresis voltage	V_{BSHY}		-	0.6	-	V
V_S quiescent negative voltage	V_{SQN}	V_B=15V	-	-5.0	-	V
Input terminal parameters						
Input high-level current	I_{IN+}	V_{IN}=5V	30	50	70	μA
Input low-level current	I_{IN-}	V_{IN}=5V	-	0	1	μA
Input high-level voltage	V_{IN+}		2.6	-	-	V
Input low-level voltage	V_{IN-}		-	-	0.8	V
Input hysteresis voltage	V_{INHY}		-	1.2	-	V
Output terminal parameters						
High-level short-circuit pulse current	I_{OUT+}	V_{IN}=5V V_O=0V PWD≤10μs	0.8	1.1	1.4	A
Low-level short-circuit pulse current	I_{OUT-}	V_{IN}=0V V_O=15V PWD≤10μs	1.5	2.0	2.5	A
High-level output voltage	V_{OUT+}	I_{OUT}=-100mA	14.20	14.48	-	V
Low-level output voltage	V_{OUT-}	I_{OUT}=+100mA	-	0.17	0.35	V
Time parameters						
Output rise edge transfer time	t_{ON}	NO Load	140	220	300	ns
Output fall edge transfer time	t_{OFF}	NO Load	140	220	300	ns
Output rise time	t_r	C_L=3.3nF	-	50	80	ns
Output fall time	t_f	C_L=3.3nF	-	23	40	ns
Dead time	DT	NO Load	210	310	410	ns
High-side/low-side matching time	MT	-	-	-	50	ns

6.7 Gate Driver (6N) Electrical Characteristics (CMS8M3536E)

6.7.1 Internal Logic Block Diagram



6N pre-driver internal logic block diagram

6.7.2 Absolute Maximum Ratings

(T_A=25˚C, unless otherwise specified, all pins are referenced to GND.)

Parameter	Symbol	Min.	Max.	Unit
High-side floating offset absolute voltage	$VB_{1,2,3}$	-0.3	225	V
High-side floating offset relative voltage	$VS_{1,2,3}$	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
High-side output voltage	$V_{HO1,2,3}$	VS1,2,3-0.3	$VB_{1,2,3}$+0.3	V
Maximum supply voltage	VCC	-0.3	25	V
Low-side output voltage	$V_{LO1,2,3}$	-0.3	VCC+0.3	V
Maximum input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	-0.3	15	V
Offset voltage maximum slew rate	dVS/dt	-	50	V/ns
Thermal resistance junction-to-ambient (Note1)	θ_{JA}	-	60	˚C/W
Junction temperature	T_J	-	150	˚C
Storage temperature	T_S	-55	150	˚C
Pin soldering temperature (duration 10s)	T_L	-	260	˚C
ESD_HBM (Note2)	V_{ESD1}	-	2000	V
ESD_CDM	V_{ESD2}	-	750	V

Note:

1) T_A represents the operating temperature at which the circuit operates, $\theta_{JA}$the thermal resistance of the package, 150˚C is the maximum operating junction temperature of the circuit.
2) For the Human Body Model (HBM), a 100pF capacitor discharges through a 1.5kΩ resistor.
3) When the operating conditions of the circuit exceed the absolute maximum ratings, it is highly likely that the circuit will be immediately damaged.

6.7.3 Recommended Operating Conditions

(T_A=25°C, unless otherwise specified, all pins are referenced to GND.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-side floating offset absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+5	$V_{S1,2,3}$+15	$V_{S1,2,3}$+20	V
High-side floating offset relative voltage	$V_{S1,2,3}$	GND-5	-	200	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{S1,2,3}$+15	$V_{B1,2,3}$	V
Supply voltage	VCC	5	15	20	V
Low-side output voltage	$V_{LO1,2,3}$	0	15	VCC	V
Input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	0	-	5	V

Note：T_A represents the operating temperature at which the circuit operates.

6.7.4 Electrical Characteristic Parameters

(T_A=25℃, V_{CC}=$V_{BS1,2,3}$=15V, $V_{s1,2,3}$=GND, unless otherwise specified, all pins are referenced to GND.)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power supply current parameters						
V_{CC} quiescent current	I_{CCQ}	V_{IN}=0V	72	81	89	uA
V_{BS} quiescent current	I_{BSQ}	V_{HIN}=0V	27	30	33	uA
V_{CC} dynamic current	I_{CCD}	$f_{LIN1,2,3}$=20kHz	300	319	360	uA
V_{BS} dynamic current	I_{BSD}	$f_{HIN1,2,3}$=20kHz	113	125	132	uA
V_B shift current	$I_{VB\_shift\_tr}$		5.6	6.0	15.0	mA
V_B floating power leakage current	I_{LK}	V_B=V_S=225V	-	-	1	uA
Power supply voltage parameters						
V_{CC} undervoltage high-level voltage	V_{CCHY+}	-	-	4.2	4.8	V
V_{CC} undervoltage low-level voltage	V_{CCHY-}	-	3.4	3.8	-	V
V_{CC} undervoltage hysteresis voltage	V_{CCHY}	-	-	0.4	-	V
V_{BS} undervoltage high-level voltage	V_{BSHY+}	-	-	3.8	4.3	V
V_{BS} undervoltage low-level voltage	V_{BSHY-}	-	3.0	3.5	-	V
V_{BS} undervoltage hysteresis voltage	V_{BSHY}	-	-	0.3	-	V
V_S quiescent negative voltage	V_{SQN}	V_{BS}=15V	-	-5.0	-	V
Input terminal parameters						
Input high-level current	I_{IN+}	V_{IN}=5V	47	50	53	uA
Input low-level current	I_{IN-}	V_{IN}=0V	-	0	-	uA
Input high-level voltage	V_{IN+}	-	2.6	-	-	V
Input low-level voltage	V_{IN-}	-	-	-	0.8	V
Input hysteresis voltage	V_{INHY}	-	-	1.0	-	V
Output terminal parameters						
High-level short-circuit pulse current	I_{OUT+}	V_{IN}=5V, V_O=0V, PWD≤ 10μs	-	1.2	-	A
Low-level short-circuit pulse current	I_{OUT-}	V_{IN}=0V, V_O=15V, PWD≤ 10μs	-	1.2	-	A
High-level output voltage	V_{OUT+}	I_{OUT}=-100mA	-	0.8	-	V
Low-level output voltage	V_{OUT-}	I_{OUT}=+100mA	-	0.3	-	V
Time parameters						
Output rise edge transfer time	t_{ON}	No Load	130	140	160	ns
Output fall edge transfer time	t_{OFF}	No Load	130	140	160	ns
Output rise time	t_r	C_L=3.3nF	47	60	73	ns
Output fall time	t_f	C_L=3.3nF	36	45	56	ns
Dead time	DT	No Load	328	350	378	ns
High-side/low-side matching time	MT	-	-	-	50	ns
V_B shift current pulse time	t_{r_width}	-	240	300	500	ns
BRK input filter time	t_{FLT}	V_{BRK}=0/5V	45	60	75	ns

BRK on time	T_{on_BRK}	V_{BRK}=5V	120	130	160	ns
BRK off time	T_{off_BRK}	V_{BRK}=0V	120	130	160	ns

6.8 Gate Driver (3P3N) Electrical Characteristics (CMS8M3512/3524)

6.8.1 Absolute Maximum Ratings

CMS8M3512 (unless otherwise specified, T_A=25℃).

Parameter	Symbol	Range			Unit
		Min.	Typ.	Max.	
Supply voltage	GVDD	8	12	16	V
Input frequency	Fin	-	-	100	KHz

CMS8M3524 (unless otherwise specified, T_A=25℃).

Parameter	Symbol	Range			Unit
		Min.	Typ.	Max.	
Supply voltage	GVDD	16	24	30	V
Input frequency	Fin	-	-	100	KHz

6.8.2 Electrical Characteristic Parameters

6.8.2.1 NMOS

(Unless otherwise specified, VDD=24V, T_A=25℃).

Parameter	Test condition	Min.	Typ.	Max.	Unit
R1 input resistor	-	40	50	60	Ω
R2 pull-down resistor	-	16	20	24	KΩ

6.8.2.2 PMOS

(Unless otherwise specified, VDD=24V, T_A=25℃).

Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{in}P*_IN input current	V_{P*_IN}=5V	0.7	0.9	1.1	mA
V_{OH} output high level	VCC=16~30V, no load	VCC-1.5	-	-	V
V_{OL} output low level	VCC=16~30V, no load	-	0.5*VCC		
tPHH rising edge delay	VDD=24V, no load	-	75	150	ns
tPLL falling edge delay		-	75	150	
tr rising edge	VDD=12V, CL=1nF	-	100	300	
tf falling edge	VDD=12V, CL=1nF	-	100	300	

6.8.3 Description of the Time Parameter Test

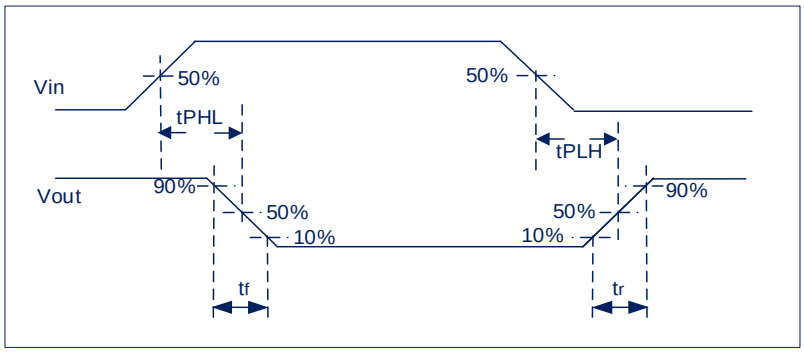
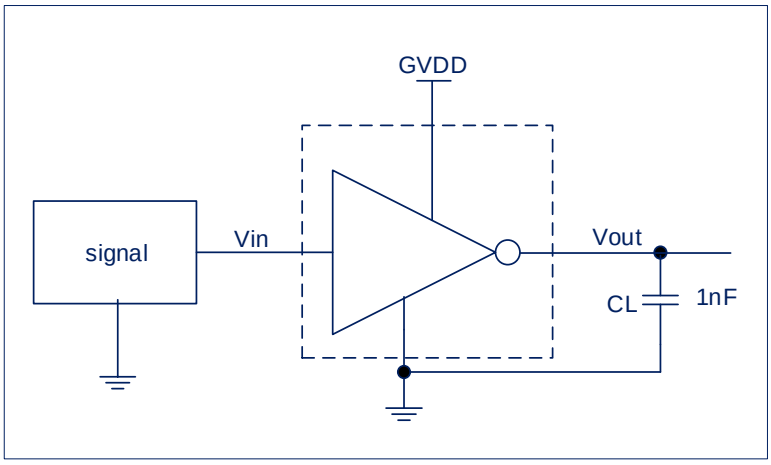
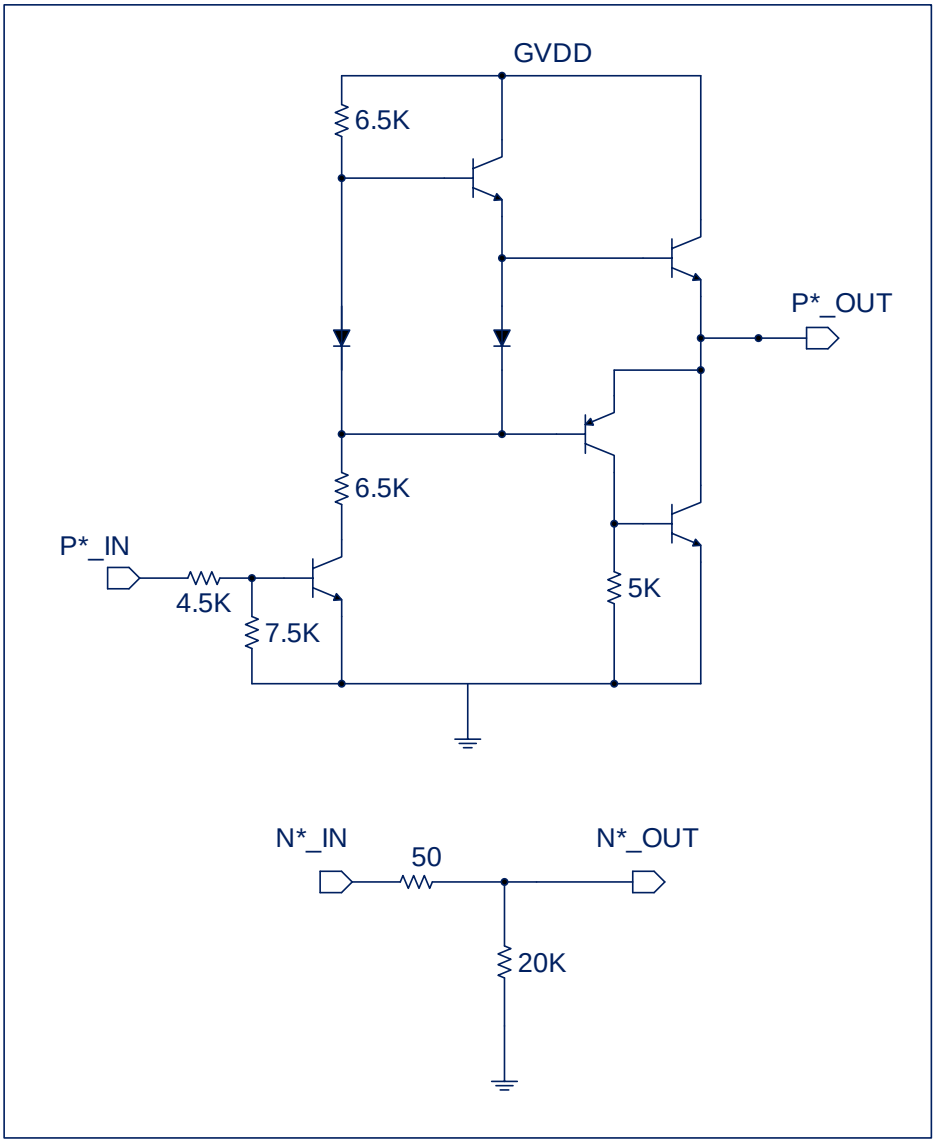


Diagram of the time parameter test



Block diagram of the test circuit

6.8.4 3P3N Pre-Driver Internal Logic Block Diagram Characteristics



3P3N pre-driver internal logic block diagram

6.8.5 Logic Truth Table

NMOS logic truth table

N*_IN	N*_OUT
Floating	L
L	L
H	H

PMOS logic truth table

P*_IN	P*_OUT
Floating	H
L	H
H	L

Note: * represents the numbers 1, 2, 3.

6.9 EMC Characteristics

6.9.1 EFT Electrical Characteristics

Symbol	Parameter	Test condition	Grade
V_{EFTB}	Fast transient voltage burst limits to be applied through 0.1uF (capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = + 25°C, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4B

Note: The immunity performance against Electrical Fast Transient (EFT) pulses is closely related to system design aspects, including power supply structure, circuit design, layout and wiring, chip configuration, program structure, and more. The EFT parameters listed in the table are results obtained from testing on CMS internal testing platforms and may not apply universally to all application environments. These test data serve as reference only. Various aspects of system design can influence EFT performance. In applications where high EFT immunity is required, it is advisable to design while minimizing the impact of interference sources on system operation. It is recommended to analyze interference paths and optimize designs to achieve the best immunity performance against EFT disturbances.

6.9.2 ESD Electrical Characteristics

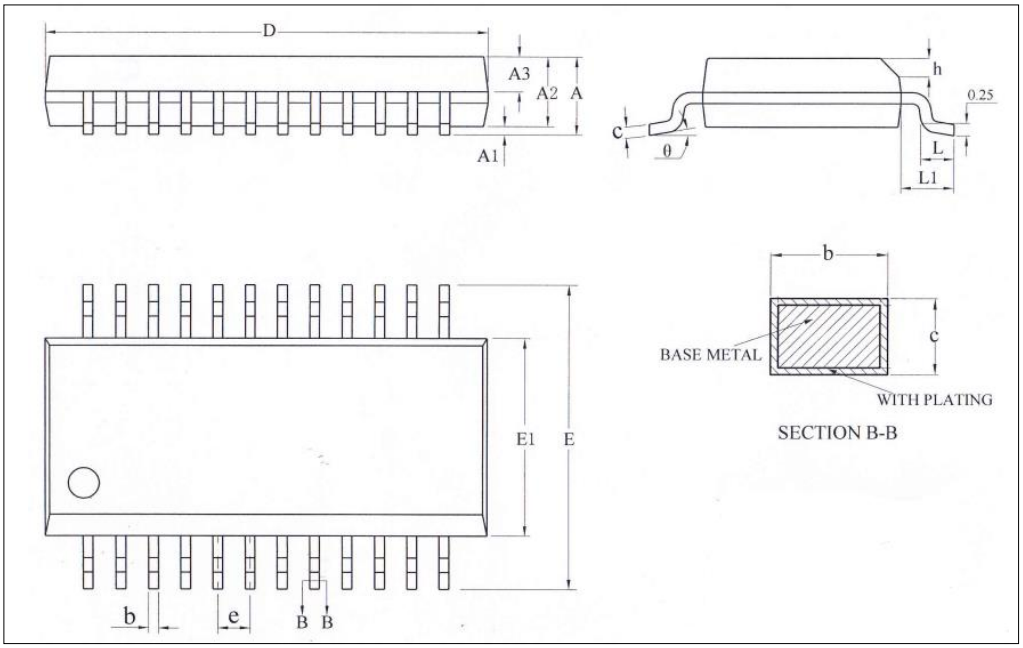
Symbol	Parameter	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human-Body Model: HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine Model: MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	C

6.9.3 Latch-Up Electrical Characteristics

Symbol	Parameter	Test condition	Classification
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)

7. Package Dimensions

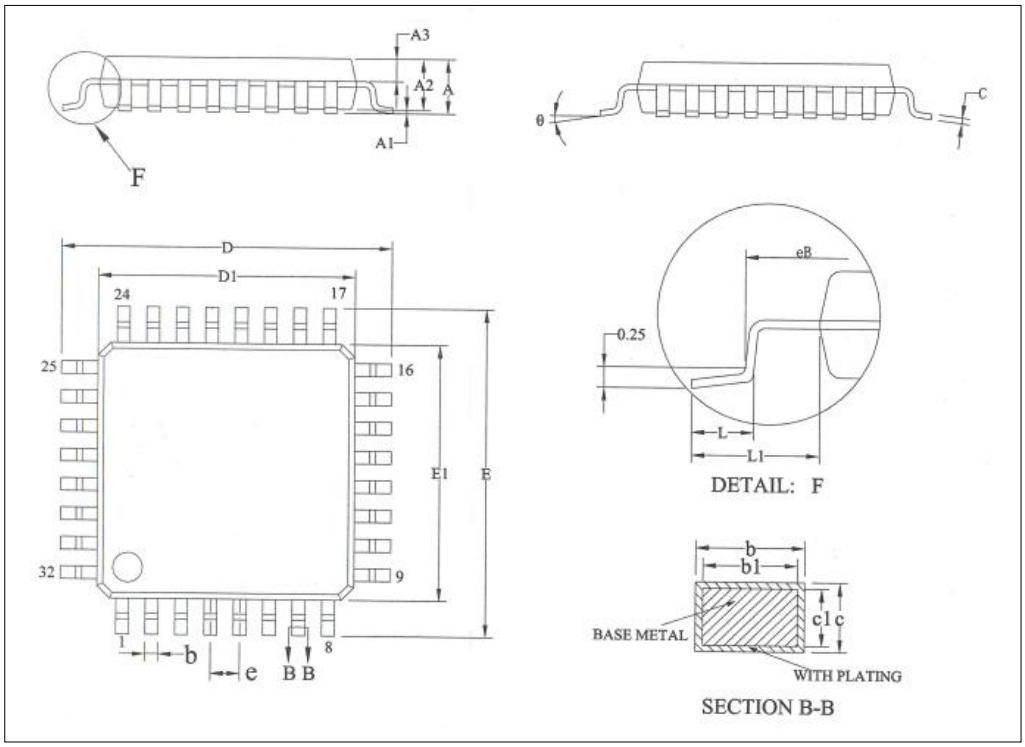
7.1 SSOP24



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.80
A1	0.10	0.15	0.25
A2	1.30	-	1.55
A3	0.60	0.65	0.70
b	0.20	-	0.31
c	0.20	-	0.24
D	8.53	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.406	-	0.889
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

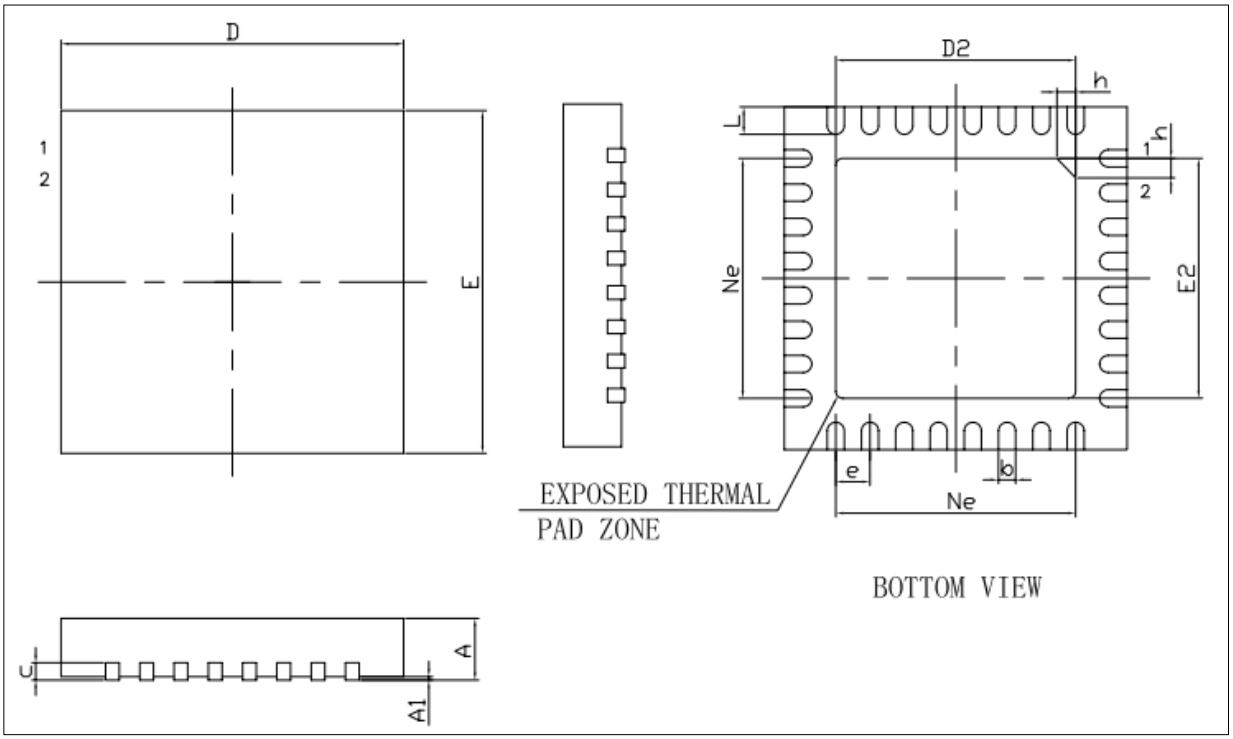
7.2 LQFP32



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
b1	0.31	0.35	0.39
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 QFN32 (5x5x0.75-0.50mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	-	3.75
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	-	3.75
L	0.30	-	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8. Revision History

Version #	Date	Description of changes
V1.00	Jan. 2020	Initial release
V1.01	Jul. 2020	Added CMS8M3524 and other chip models.
V1.02	Aug. 2020	Added CMS8M3510 and other chip models.
V1.03	Nov. 2020	Added CMS8M3512S024 and CMS8M3536L032 chip information
V1.04	Nov. 2021	Modified the chip information, added CMS8M3535 chip information.
V1.05	Jan. 2022	Modified FLASH electrical parameters
V1.06	Feb. 2022	Modified Revision History and some product descriptions.
V1.07	Feb. 2022	Modified the description of the PGA
V1.0.8	Aug. 2023	1) 6.1 Absolute Maximum Ratings: added notes to limit parameters. 2) 6.3.1 Power-On Reset Time: modified parameters 3) 6.3.3 Internal Oscillator: modified parameters 4) 6.5.1 BANDGAP Electrical Characteristics: refined parameters 5) 6.5.2 ADC Electrical Characteristics: ADC clock period is described according to different reference voltages. 6) Updated 6.8 EMC characteristics. 7) Corrected 7.2 package dimensions
V1.0.9	Mar. 2024	Added CMS8M3510S024 model and related information
	May 2024	Added CMS8M3536EQ032 model and related information
V1.1.0	Jul. 2024	Corrected 2.2.3 Memory Address
	Oct. 2024	Corrected SSOP24/LQFP32/QFN32 package dimensions.
V1.1.1	Dec. 2024	Added notes to section 6.5.2
V1.1.2	Jan. 2025	1) Removed CMS8M3535 model and related information. 2) Added 6.6.1 Internal Logic Block Diagram. 3) Modified section 6.6.2/6.6.3/6.6.4/6.7.2/6.7.4/6.8.2.2 parameters.